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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jeffrey S. Mailloux et al.

Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

Docket No.: 303.623US1
Filed: May 20, 1996
Examiner: Hong Kim

Serial No.: 08/650,719
Due Date: August 9, 2004
Group Art Unit: 2186

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is presented in response to the Office Action (Paper 48) mailed on May 7, 2004, wherein prosecution of the above-identified Application was re-opened in response to the Appeal Brief filed by the Appellants on January 14, 2004. It is respectfully requested that the Appeal be reinstated as permitted by M.P.E.P. § 1208.02. This Supplemental Appeal Brief is to be considered a response to the Final Rejection of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 in the above-identified Application, as set forth in the Final Office Action mailed on May 13, 2003, as well as to the rejection of the same claims in the Office Action mailed on May 7, 2004. No new amendments, affidavits, or other evidence has been submitted.

This Supplemental Appeal Brief is filed in triplicate. No new fees should be necessary, as noted in M.P.E.P. § 1208.02. The Appellants respectfully request reconsideration and reversal of the pending claim rejections.

APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are four appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. These related appeals are currently pending before the Board and concern U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2), U.S. Patent Application Serial Number 08/984,562 (Atty. Ref. No. 303.623US3), U.S. Patent Application Serial Number 08/984,563 (Atty. Ref. No. 303.623US4), and U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). A fourth, related appeal was also pending with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowability indicating allowance of all claims was mailed to the Appellants (Paper 32), the application has now issued as U.S. Pat. No. 6,615,325, and this matter is no longer before the Board.

3. STATUS OF THE CLAIMS

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are currently pending, and the rejection of these claims is appealed. A list of the pending claims is included as Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Supplemental Response to the Second Final Office Action mailed to the Appellants on March 15, 2002, in which claim 7 was amended to correct a typographical error.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, the embodiments disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, an asynchronously addressable storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). Some embodiments can switch between burst access and pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In the pipelined mode, multiple switching modes are possible, including both row-based and column-based switching. (Pg. 9, lines 5-9). In addition to the embodiments described herein, other embodiments of varying scope, such as systems, methods, and storage devices, including memory circuits, are disclosed. (Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1) Whether claim 61 was properly rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

2) Whether claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter "Manning").

3) Whether claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were properly rejected under 35 USC § 103(a) as being obvious over Manning in view of U.S. Patent No. 6,065,092, issued to Roy (hereinafter "Roy").

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this Appeal.

8. ARGUMENT

a) The Applicable Law

To make out a *prima facie* case of lack of written description under the first paragraph of 35 U.S.C. § 112, four elements must be shown:

1) The application does not reasonably describe or convey the concepts
2) to one of ordinary skill in the art
3) at the time of filing the patent application
4) of the claimed invention.

It is respectfully noted that "[i]f even one of these elements of the prima facie case is not present, the rejection is improper and must be withdrawn." *See* Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002. Since "[t]he initial burden is on the PTO to establish that the now claimed subject matter is not described by the specification ...", the Office must show why this element is not sufficiently described in the application as to each element of the prima facie case. *Id.*, citing *Ex parte Anderson*, 21 U.S.P.Q. 2d 1241 (B.P.A.I. 1991).

Establishing anticipation under 35 USC § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co.*

of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be

presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.,* 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record. The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

b) The References

Manning teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of how to apply the architecture, or its operation, are given.

Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. (Col. 26, lines 62-66). New actions may be initiated when a burst is completed. (Col. 27, lines 4-14). The device may also be used in a pseudo-pipelined access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. (See Col. 28, lines 16-32 and Col. 33, lines 8-19). While limited access pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. (Col. 33, lines 65-67). The Appellants were unable to find any indication that Roy enables selecting true pipelined and burst operation "on the fly" as demonstrated by the disclosed embodiments (due to restriction imposed by software header mode changes and channel data/address sharing). For example, row-based switching operation is not possible (i.e., "... cannot be used to change a row in every cycle ..."). (Col. 38, lines 23-24).

c) Discussion of the Rejections

***c.1* -- The rejection under § 112:**

Claim 61 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. It has also been requested that this feature be added to the drawings. Because a *prima facie* case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as-filed, the Appellants respectfully traverse this rejection.

It is asserted in the Office Action that the limitation "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" was not described in the specification. Merely asserting that a particular embodiment has been described, and noting that claim 61 does not cover that particular embodiment does not take into account the numerous other embodiments that have been described, both in the application text, and in the figures. In other words, FIG. 17 and claim 46 are not to be considered as effectively limiting all possible embodiments. Rather, this figure and claim are merely illustrative one some of the many possible embodiments.

To demonstrate that the limitation is indeed present in the Application, the Appellants have made numerous references in other responses to the following Application text: pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. The attention of the reader is now also directed to pg. 33, lines 13-21 and pg. 38, lines 11-15 of the Application. In these passages it is noted that some embodiments enable "using an initial externally generated address followed by one or more internally generated addresses" as well as "switching between burst access ... and ... pipelined modes of operation without ceasing." Finally, as noted on pg. 27, lines 5-11, "After a first /CAS signal 114 cycle in burst mode which uses the initial external values supplied for addresses XA0 and XA1, counter 149 increments those initial values and provides new internally generated addresses A0 and A1 by supplying count 0 signal 140 and count 1 signal 141 to respective A0 and A1 locations in temporary storage 119 through MUXs 125, 124. In this manner, internal addresses may be generated based on an initial external address."

Given the wide variety of described embodiments, it should be clear that if a pipelined mode is selected prior to entering the burst mode, with an external address supplied, and then the burst mode is selected thereafter, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" is indeed possible.

In addition, it is respectfully noted that "An application need not contain a word-for-word description of the claimed invention to satisfy the written description requirement. ... All that is needed is that the application reasonably convey the claimed subject matter." See Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002. Given the written description, and the activity of the embodiments described with respect to selecting true pipelined and burst modes (which is not permitted by the cited art), the limitation "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" has indeed been described in multiple ways as a part of the Application as-filed.

As noted in Section 8(a) above, to establish a prima facie case of lack of written description under § 112, each one of four elements must be demonstrated. Viz, (1) the application does not reasonably describe or convey the concepts (2) to one of ordinary skill in the art (3) at the time of filing the patent application (4) of the claimed invention. None of the elements has been shown.

Therefore, since a prima facie case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as filed, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

Finally, it is noted that an objection to Claim 61 has been raised due to a perceived informality. The Office Action noted that it appeared the terms "burst" and "pipelined" should be interchanged so that claim 61 was "consistent" with claim 46. However, it seems this request arises from a fundamental misunderstanding of the operations enabled by various embodiments, and thus, amending claim 61 is not necessary. The activities noted in the claim are not necessarily accomplished in the order shown, or in any particular order. As noted previously, some of the disclosed embodiments can make use of external addresses in one mode that were initially supplied while in another mode. For example, the following arrangement of the claim elements may also be used (the terminology has not been changed at all – the elements have merely been placed in a different order):

61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;

selecting a pipeline mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation;

switching modes to the burst mode of operation; and

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.

If desired, the Examiner may effect an Examiner's amendment so that claim 61 is worded as shown above; the meaning of the claim is exactly the same, but may appear to have additional clarity. The terminology used in the claim is correct and arises from the unique operating qualities of the disclosed embodiments (e.g. being able to change from burst to pipelined modes "on the fly", which none of the cited references disclose, and making use of initial addresses supplied in other

modes). Thus, if such an amendment is effected, it will be for reasons of Examiner preference, and not for reasons related to patentability.

***c.2* -- The rejection under § 102:**

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, the Appellants respectfully traverse this rejection under 35 USC § 102(e).

c.2.1. *Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims* .

Manning specifically fails to disclose "circuitry ... configured to switch between the pipelined mode and the burst mode" as claimed by the Appellants in claim 1. Similarly, Manning fails to disclose that the burst mode and the pipelined mode are "extended data out modes" (claims 2-4); or that the "pipelined/burst mode circuitry" includes: a "buffer for storing an (external) address", a "counter for incrementing an address", "is coupled for receiving an external address", or"multiplexed devices for providing an internally generated address" (claims 5-9).

Further, Manning does not teach "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes (claims 33-34, 46, 59-61); much less how addresses are supplied while selecting or switching modes (claim 35), or what type of switching environment may be used in burst and pipelined modes of operation (claims 48-49). Finally, Manning does not describe a system including a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode", or a storage device/memory including circuitry "switchable between burst and pipeline modes of operation" (claims 50, and 63-64).

Several assertions were made in the Office Action, attributing support to various concepts allegedly disclosed by Manning. However, a careful reading of each citation reveals that the discussion of the asserted elements is incorrect. These assertions have been made with respect to:

Claims 2, 3 - Manning does not disclose that the pipelined mode is an EDO mode of operation (the two concepts are never discussed in conjunction with each other).

Claim 9 - Manning does not disclose mode selection circuitry which includes a multiplexed device (the components referenced in the Office Action are an address counter 26 and a column address decoder 30).

Claim 34 - Manning does not disclose switching between the pipelined mode and the burst mode (Manning merely refers to the possibility of using a pipelined architecture).

Claim 35 - Manning does not disclose selecting an external address along with selecting between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 48, 49 - Manning does not disclose several switching environments in conjunction with burst and pipelined modes (Manning merely refers to the possibility of using a pipelined architecture).

Two more erroneous assertions are directed toward all pending claims. First, it is not true that one must "select pipeline mode" to "work in the pipeline architecture". The assertion is erroneous because the pipelined mode does not need to be selected if a device always operates in that mode (e.g., the EDO burst mode, with a pipeline architecture, as explained below). Thus, the statement in the Office Action that "it is inherent that the memory selectively operable in a pipelined mode because in order to work in a standard EDO memory including a pipeline architecture, [sic] one has to select a pipeline EDO mode" is simply incorrect. Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward a single device, accessing a single device, accessing different locations in a single device, or a single device included in a system.

c.2.2. *Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim .*

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support switching or selecting between

burst and pipelined modes of operation, as claimed in claims 1, 33, 46, 50, 59-61, and 63-64 (and in all claims that depend from them)?

Second, the Office has failed to produce a *prima facie* case of anticipation. While the assertion is made that Manning discloses "mode circuitry to select between a burst mode and a pipelined mode", and that the circuitry is "configurable to select between [the] two modes", the Appellants' representative, after a careful study of Manning, was unable to locate any such selection circuitry, nor any aspect of such circuitry which was configurable to select between burst and pipelined modes of operation.

Finally, the Office has admitted the deficiencies of Manning in a related matter with respect to several elements claimed by the Appellants in the instant Application. The attention of the Office is directed to the following assertions made by the Appellants in the appeal of U.S. Application Serial No. 08/984,561:

> "Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to select or switch between burst and pipelined modes of operation..." (emphasis added)

This language was approved by the Office in a subsequent Notice of Allowability (Paper 32) mailed to the Appellants on March 21, 2003. In this Notice, the Office states:

> "The claims are allowable over the prior art of record because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth in claims 1-23."

Thus, the Office has approved statements by the Appellants in a related matter to the effect that Manning simply does not teach switching or selecting between the pipelined mode and other modes of operation.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the true pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal*

addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory improves EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by

the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id. Roy alludes to this type of mechanism, where burst EDO operation is described as being one step below "[a] more sophisticated evolutionary approach to achieving a higher pipelined bandwidth ..." involving synchronous DRAM. Roy, Col. 4, line 58 – Col. 5, line 6.

As a matter of contrast, in some embodiments of the Appellants' invention, a newburst signal from control logic is provided. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with a stored initial external address. A counter is then used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through the memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13). Column-based access, as well as row-based access are possible. (Application, Pg. 9, lines 5-9).

Thus, Manning simply does not disclose any method or device for switching between burst and pipelined modes of operation. What is discussed by Manning is not identical to the subject matter of various embodiments of the invention as required by the M.P.E.P., and the rejection is under § 102 is therefore improper. Therefore, reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

c.3 – The rejection under 35 U.S.C. 103 :

First, the Appellants do not admit that Manning or Roy are prior art and reserve the right to swear behind these references in the future. Second, because each of the references fails to teach

the element of switching between true pipelined and burst modes of operation, and because there is no motivation to combine the references in the record, the Appellants respectfully traverse this rejection under § 103 by the Office.

The Appellants are unable to find how Manning or Roy, in any combination, serve to teach the invention of independent claims 1, 33, 46, 50, 59-61, and 63-64. As noted previously, and as admitted by the Office, Manning does not disclose selecting, choosing, or switching between burst and pipelined modes of operation. It is also known that Roy, at best, teaches pseudo-pipelined operation. In other words, Roy permits pipelined reads, as long as they are confined to a single row. See Roy, Col. 38, lines 17-37. This is in direct contrast to the teachings of the Appellants, which enable true piplelined operation, with column-based switching in addition to row-based switching (See Application, pg. 38, lines 7-16). Similarly, Roy's pseudo-pipelined writes may only occur at up to half the channel speed, since data and addresses are shared on the channel. Roy, Col. 39, lines 6-24. The Appellants disclosed embodiments do not suffer from this limitation. Thus, none of the references disclose switching between burst and true pipelined modes of operation. Since it is therefore a logical impossibility for any combination of the references to disclose this aspect of the invention, a *prima facie* case of obviousness can not be established.

These conclusions apply with even greater force with respect to dependent claims 2-9, 34-35, and 48-49, since each one includes additional, patentable features over those delineated in the independent claims. If an independent claim is nonobvious under 35 USC § 103, then any claim depending therefrom is nonobvious. See M.P.E.P. § 2143.03.

Even so, many assertions are made in various Office Actions respecting the instant Application to the effect that Manning discloses switching or changing modes to a pipelined mode (even to the extent of specifying where in the cycles of a memory operation the change to a pipelined mode occurs (see Paper 24, Page 11, regarding claim 67). However, the Appellants' representative can find no such teaching in Manning. And while Roy teaches the ability to change modes, the change occurs due to header-prompted pseudo-pipelined operation, and header-prompted burst modes, for example.

No reply has been received by the Appellants in response to repeated requests for more specific citations in Manning as to precisely how such activity is enabled by the references, and this is not surprising, because, as noted above, the Office agrees that "*Manning does not specifically*

disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." However, the Office continues to set forth the single statement in Manning (col. 5, lines 43-50) which alludes to the possible existence of a pipelined architecture as somehow providing a basis for switching between burst and pipelined modes. In fact, this text provides no description whatever as to how such an implementation might be accomplished - especially with regard to changing between a pipelined mode and other operational modes at will, in the same memory, using individual operational signals, as disclosed and claimed by the Appellants. Manning Col. 6, lines 14-34 describes burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and true pipelined modes of operation, as claimed by the Appellants. Neither does Roy.

Thus, since no mention is made in any of the references to switching, selecting, or choosing between burst and true pipelined modes of operation, combining Manning with Roy does not result in a device having asynchronously selectable burst and pipelined modes of operation (i.e., true pipelined operation, with both row-based and column-based switching available). It is only hindsight gained from the Appellants' disclosure which enables providing both burst and true pipelined modes of operation in a single memory device, and switching therebetween at will.

The Office asserts that Manning and Roy should be combined because "the memory access performance of Manning would been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle ...". However, this assertion overlooks the pseudo-pipelined access limitations of Roy, namely: (1) read operations are confined to the same row (no row-based switching), and (2) write operations only occur at one-half the channel speed; not at the full speed of the channel.

Further, combining Roy with Manning also overlooks the following statement in Manning: "An integrated circuit memory device is designed for high speed data access and compatibility with *existing* memory systems." (Manning, Abstract, emphasis added). The device is made to be compatible with existing systems; not radically new systems, such as that described by Roy, in which "[o]ne of the fundamental features of this architecture is the use of the same lines of a data channel for both address and control information, as well as for bi-directional data transfers. Data

read and write operations within the memory device are organized into discrete "transactions," with each such transaction initiated by several sequential data words termed a "header." The header includes address and control information for a subsequent transfer of one or more bytes of data into or out of the memory device. The header can be applied to one channel for a subsequent transaction across that same channel or across another channel." Thus, Manning teaches away from the asserted combination, since the two devices are fundamentally incompatible. Therefore, since there is no evidence in the record to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is actually using personal knowledge, and the Examiner is respectfully requested to submit an affidavit supporting such knowledge as required by 37 C.F.R. § 1.104(d)(2).

In closing, since each of the cited references fail to teach all aspects of the Appellants' invention as claimed, since no combination of the references can be made which teaches these aspects, and since there is no motivation in the record to combine these references, the Appellants respectfully assert that no prima facie case of obviousness has been established, and therefore request reconsideration and withdrawal of the rejection with respect to claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 under 35 U.S.C. §103.

c.4 -- Why the claims are separately patentable :

While the separate patentability of each claim has been discussed in the "Argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 1 is directed toward an asynchronously-accessible storage device having "mode circuitry configured to switch between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or pipelined mode ... for operating the asynchronously-accessible storage device in either mode." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 1, dependent claim 2 adds "the burst mode and the pipelined mode are extended data out modes of operation." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 3 adds "the pipelined mode is an extended data out mode." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 4 adds "the burst mode is an extended data out mode." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 5 adds "the pipelined ... mode circuitry includes a buffer ... for storing an address." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim (except claim 6) has this unique combination of elements. To the elements of dependent claim 5, dependent claim 6 adds "the pipelined ... mode circuitry includes at least one counter ... for incrementing the address." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 7 adds "the pipelined ... mode circuitry is coupled for reading an external address." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim (except claims 8 and 9) has this unique combination of elements. To the elements of dependent claim 7, dependent claim 8 adds "the pipelined ... mode circuitry includes a buffer ... for storing the external address." To the elements of dependent claim 7, dependent claim 9 adds "the pipelined ... mode circuitry includes multiplexed devices for providing an internally generated address to the storage device." Neither Manning nor Roy, nor any combination of these two references discloses these combinations of elements, and no other claims have these unique combinations of elements.

Independent claim 33 is directed toward a method of accessing a storage device comprising "receiving a first address", "obtaining a second address", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode" and "asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address." Neither Manning nor Roy, nor any

combination of these two references discloses this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 33, dependent claim 34 adds "switching between the burst mode and the pipelined mode." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 33, dependent claim 35 adds "the second address is an external address." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 46 is directed toward a method of accessing a storage device comprising "selecting a pipelined mode of operation", "providing a new external address for every access associated with asynchronously accessing the ... device while in the pipelined mode of operation", and "switching modes to a burst mode of operation". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 46, dependent claim 48 adds "the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching." Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 46, dependent claim 49 adds "the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 50 is directed toward a system including "a microprocessor" and "a memory coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory". Neither Manning nor Roy, nor any combination of these two references discloses this combination

of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

Independent claim 59 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal", and "accessing a storage element ... in the selected mode of operation". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 60 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between outputting information ... and inputting information", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal" and "asynchronously accessing a storage element ... in the selected mode of operation". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 61 is directed toward a method of accessing a storage device comprising "selecting a pipeline mode of operation", "providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation", "switching modes to the burst mode of operation", and "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 63 is directed toward a storage device having "an array of memory cells" and "mode circuitry for receiving a burst/pipeline signal". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

Independent claim 64 is directed toward a memory circuit having "an array of memory cells" and "burst/pipeline selection circuitry for determining a burst or a pipeline mode of

operation". Neither Manning nor Roy, nor any combination of these two references discloses this combination of elements, and no other claim has this unique combination of elements.

c.5 – The double patenting rejection :

Claims 59 and 60 were provisionally rejected under the judicially created doctrine of double patenting over claim 36 of co-pending Application No. 08/984,563. Claim 61 was provisionally rejected under the judicially created doctrine of double patenting over claim 59 of U.S. Pat. No. 6,615,325.

Co-pending U.S. Patent Application Serial No. 08/984,563 has not yet received any final indication of allowed claims. The Appellants request that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Appellants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

The Examiner has compared claim 61 of the instant application to claims 1-23 of U.S. Pat. No. 6,615,325, and determined that a judicially-created non-statutory double patenting rejection is required. This being the case, the Appellants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon receiving an indication of allowance for claim 61 in the instant application.

9. SUMMARY

It is respectfully submitted that claim 61 is indeed supported by the subject matter contained in the Application as-filed, and that a *prima facie* case of lack of written description under 35 U.S.C. §112 has not been established. Further, no *prima facie* case of anticipation or obviousness with respect to claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 has been established under either 35 U.S.C. §102 or 35 U.S.C. §103, respectively. Therefore, reconsideration and withdrawal of the rejections of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also requested. The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6951

Date August 9, 2004 By _____

Suneel Arora
Reg. No. 42,267

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief- Patents, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of August 2004.

Name Tina Kohut

Signature

APPENDIX I

The Claims on Appeal

1. An asynchronously-accessible storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode; and

circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.

2. The asynchronously-accessible storage device of Claim 1 wherein the burst mode and the pipelined mode are extended data out modes of operation.

3. The asynchronously-accessible storage device of Claim 1 wherein the pipelined mode is an extended data out mode.

4. The asynchronously-accessible storage device of Claim 1 wherein the burst mode is an extended data out mode.

5. The asynchronously-accessible storage device of Claim 1 wherein the piplined/burst mode circuitry includes a buffer, the buffer for storing an address.

6. The asynchronously-accessible storage device of Claim 5 wherein the piplined/burst mode circuitry includes at least one counter for incrementing the address.

7. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst mode circuitry is coupled for reading an external address.

8. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes a buffer for storing the external address.

9. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes mutliplexed devices for providing an internally generated address to the storage device.

33. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device;

selecting between outputting information from the storage device and inputting information to the storage device;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

34. The method of Claim 33, further comprising switching between the burst mode and the pipelined mode.

35. The method of Claim 33, wherein the second address is an external address.

46. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipelined mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined mode of operation;

switching modes to a burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation.

48. The method of Claim 46 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 46 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and

a system clock coupled to the microprocessor.

59. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

60. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between outputting information from the storage device and inputting information to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipeline mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;

switching modes to the burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation; and

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.

63. A storage device, comprising:

an array of memory cells;

mode circuitry for receiving a burst/pipeline signal; and

operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation.

64. A memory circuit, comprising:

an array of memory cells;

burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit; and

mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.

APPENDIX II

Reference

"Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999.

Company

Shuttle

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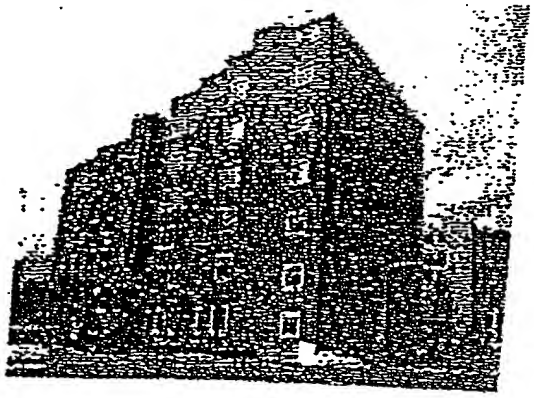

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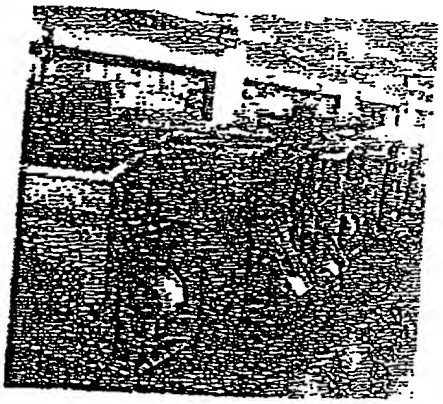

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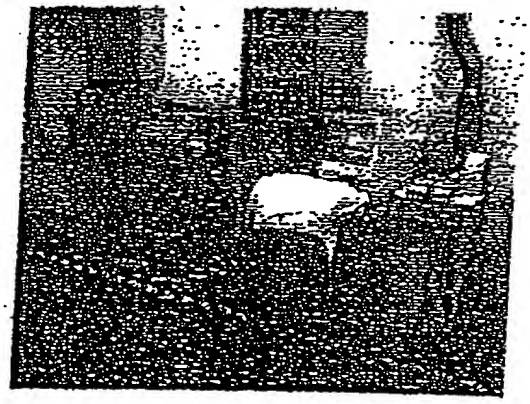

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Our company is a member of the global together with the whole global enterprises t the green environment. We are dedicated protection of the environment and the environmental pollution, for the minimizing of handling of energy conservation, as well as to related legal requirements. This is to allow th be able to have our manufactured green p eventually protect our environment.

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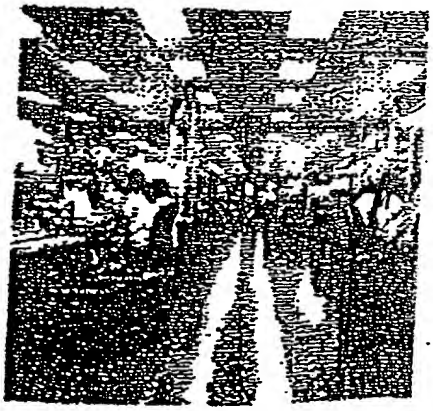
- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products



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SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

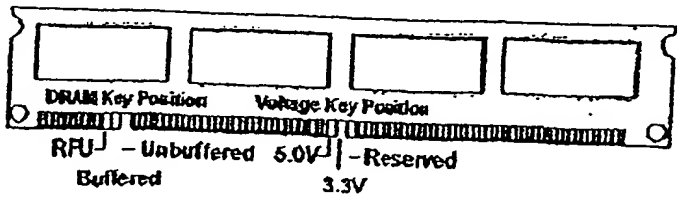
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

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